WHAT IS CLAIMED IS:

1. A method for deplating defective capacitors comprising:

forming a plurality of capacitors on a semiconductor substrate;

forming a plurality of metal contacts on the plurality of capacitors;

depositing a layer of photoresist on the semiconductor substrate;

patterning the photoresist layer so that the plurality of metal contacts are exposed;

contacting the exposed metal contacts with an electrically conductive solution; and

deplating metal contacts which are disposed over defective capacitors.

2. The method of Claim 1 wherein the defective capacitors comprise capacitors having at least one short circuit.

3. A method for forming a multi-chip module comprising:

forming a thin-film polymeric interconnect structure having a first side and a second side disposed on a silicon substrate which includes active or passive devices; and

mounting a computer chip on the first side of the thin film interconnect structure.

4. The method of Claim 3 further comprising reducing the thickness of the semiconductor substrate to form a thin semiconductor layer, and then forming an aperture through the thin semiconductor layer.

5. The method of Claim 3 further comprising disposing a ceramic carrier on the semiconductor layer on the side opposite the interconnect structure.

6. A multi-chip module comprising:

a thin-film polymeric interconnect structure having a first side and a second side;

a chip disposed on the first side;

a semiconductor layer disposed directly on the second side and including active or passive devices.

7. The multi-chip module of Claim 6 wherein the active devices comprise SRAMs and wherein the passive devices comprise chip capacitors.

8. The multi-chip module of Claim 6 wherein the semiconductor layer further comprises an aperture extending through the layer.

9. The multi-chip module of Claim 8 wherein the aperture is filled with solder.

10. A multichip module substrate capacitor structure comprising:

a substrate having a top surface and a bottom surface;

a doped region of the substrate located at the substrate's top surface;

an ohmic contact located on the top surface of the substrate, and a first dielectric layer disposed over the doped region;

a first conductive layer having a top surface and a bottom surface, and being disposed over the first dielectric layer with its bottom surface adjacent to the first dielectric layer, said first conductive layer having at least a sub-layer of a first conductive material disposed at its top surface;

a second dielectric layer disposed over the first conductive layer;

an aperture formed in the second dielectric layer and disposed over the first conductive layer to expose a portion thereof;

a conductive via formed through the aperture and disposed against a portion of the first conductive layer and comprising a second conductive material disposed adjacent to the sub-layer of first conductive material of said first conductive layer, said second conductive material being different from said first conductive material; and

a second conductive layer having a top surface and a bottom surface, and being disposed over the second dielectric layer with its bottom surface adjacent to second dielectric layer, said second conductive layer having a portion therefor disposed over the conductive via.

11. The module of Claim 10 wherein said first conductive layer comprises polysilicon and a top layer of aluminum.

12. The module of Claim 10 wherein the doped region comprises a top dope layer formed over substantially the entire surface of the substrate.

13. The module of Claim 10 wherein said substrate comprises a doping level of more than 1 x $10^{-18}cm^{-3}$ and wherein the doped region is provided by the entire substrate.

14. The module of Claim 10 wherein said first dielectric layer comprises silicon oxide.